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METHOD FOR GENERATING A COMMAND FILE OF A GROUP OF DRC RULES AND/OR A COMMAND FILE OF A GROUP OF LVS/LPE RULES

Abstract

A method is capable of generating a command file of a group of design rule check (DRC) rules or layout versus schematic (LVS) rules and layout parasitic extraction (LPE) rules that can be used by a layout verification tool to verify the layout and the parasitic characteristics of an integrated circuit. The method comprises choosing whether to generate a command file of DRC rules or a command file of LVS/LPE rules, selecting a process from a group of processes, setting a set of parameters, and extracting program codes from a plurality of modules according to the selected process and the set of parameters so as to generate a command file of DRC rules or LVS/LPE rules.